CERTIFICATE

I, Takumi SASAKI, residing at 1-11-11, Higashi-oowada, Ichikawa-shi, Chiba-ken, 272-0026 Japan, hereby certify that I am the translator of the attached document, namely a Certified Copy of Japanese Patent Application No. 2000-390166 and certify that the following is a true translation to the best of my knowledge and belief.

Takumi Sasaki February 9, 2006

Signature of Translator Date

[Name of Document] Application for Patent

[Reference No.] P1914EP

[Date of Filing] December 22, 2000

[Addressee] Commissioner of the Patent Office

[Int. Cl.] H01L 21/02

[Int. Cl.] G03F 1/00

[Inventor]

[Address] c/o Seiko Epson Corporation, 3-5, Owa 3-chome, Suwa-shi, Nagano-ken

[Name] Mitsuru SATO

[Inventor]

[Address] c/o Seiko Epson Corporation, 3-5, Owa 3-chome, Suwa-shi, Nagano-ken

[Name] Yoshiaki MORI

[Applicant for Patent]

[Id. No.] 000002369

[Name] Seiko Epson Corporation

[Agent]

[Id. No.] 100091306

[Patent Attorney]

[Name] Tomokazu MURAKAMI

[Sub-agent]

[Id. No.] 100086922

[Patent Attorney]

[Name] Misao OHKUBO

[Application Fees]

[Prepayment Registration No.] 002196

[Amount of Payment] 21000

[List of Documents Attached]

[Name of Document] Specification 1

[Name of Document] Drawings 1

[Name of Document] Abstract 1

[Proof] Required

[Name of Document] SPECIFICATION

[Title of the Invention] PATTERN FORMING METHOD AND SEMICONDUCTOR DEVICE MANUFACTURED BY THE METHOD

[Claims]

[Claim 1] A method for forming a pattern comprising the steps of forming an organic layer on a surface of a work-piece, forming a recessed portion having a predetermined pattern in the organic layer, filling the recessed portion with an inorganic material, removing the inorganic material except for the part where the inorganic material is located in the recessed portion, and removing the organic layer to allow the pattern comprising the inorganic material to remain.

[Claim 2] The method for forming a pattern according to Claim 1, wherein the filling of the recessed portion with the inorganic material is performed by applying a solution containing the inorganic material onto the recessed portion.

[Claim 3] The method for forming a pattern according to Claim 2, wherein the inorganic material is in a liquid phase or in a gas-liquid mixed phase.

[Claim 4] The method for forming a pattern according to Claim 2 or 3, wherein the application of the inorganic material is performed by a spin coating method.

[Claim 5] The method for forming a pattern according to Claim 2 or 3, wherein the application of the inorganic material is performed by a spraying method.

[Claim 6] The method for forming a pattern according to Claim 1,

wherein the removal of the inorganic material except for the part where the inorganic material is located in the recessed portion is performed by applying an etching solution.

[Claim 7] The method for forming a pattern according to Claim 6, wherein the etching solution is in a liquid phase or in a gas-liquid mixed phase.

[Claim 8] The method for forming a pattern according to Claim 6 or 7, wherein the application of the etching solution is performed by a spin etching method.

[Claim 9] The method for forming a pattern according to Claim 6 or 7, wherein the application of the etching solution is performed by a spraying method.

[Claim 10] The method for forming a pattern according to Claim 1, wherein the removal of the inorganic material except for the part where the inorganic material is located in the recessed portion is performed by a CMP method.

[Claim 11] The method for forming a pattern according to Claim 1, wherein the organic layer is removed by an atmospheric pressure plasma process.

[Claim 12] A semiconductor device manufactured by a method for forming a pattern according to any one of Claims 1 to 11.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention generally relates to a method for

manufacturing semiconductor devices, liquid crystal devices, and other devices having thin-films, and particularly relates to a method for forming a pattern under substantially atmospheric pressure without using vacuum means during the manufacturing of devices and relates to a semiconductor device manufactured by this method.

[0002]

[Description of the Related Art]

Conventionally, in a process of manufacturing a semiconductor device, elements are formed on a substrate and a wiring pattern layer is then formed above the elements.

FIGS. 10 and 11 are illustrations each showing successive steps of a conventional patterning process. When, for example, wiring is provided on a semiconductor wafer 1 shown in FIG. 10 (1) having an insulating layer, not shown, a wiring layer 2 is formed on a layer above the semiconductor wafer 1 by a plasma CVD method, as shown in FIG. 10 (2). The wiring layer 2 may be formed by a sputtering method.

[0003]

After forming the wiring layer 2 on the layer above the semiconductor wafer 1 in the above manner, a photoresist is applied onto the wiring layer 2 to form a resist layer, and the resulting resist layer is subjected to an exposure step and is then subjected to a photo-etching step to pattern the resist layer 3, as shown in FIG. 10 (3).

[0004]

As shown in FIG. 11 (1), the semiconductor wafer 1 is subjected to a dry etching step to etch the wiring layer 2 using the resist layer 3

as a mask. This situation is shown in FIG. 11 (2). In the state that a part of the wiring layer 2 only under the resist layer 3 remains, the resist layer 3 on the wiring layer 2 is removed using a solvent.

Through these steps, wiring is completed on the semiconductor wafer 1.

[0005]

[Problems to be Solved by the Invention]

However, in the above manufacturing method and a semiconductor device manufactured by the method, there are the following problems.

In conventional processes, since almost all the steps require a vacuum environment (reduced pressure environment), a vacuum system is essential to the processes. The vacuum system and a utility system such as an exhaust system and a water-cooling system working for maintaining the operation of the vacuum system consume a large quantity of energy, which corresponds to 60% or more of the energy consumed in a manufacturing process. This is a serious problem.

[0006]

For a CVD system used for forming an insulating layer, it is necessary to use PFC gases such as CHF_3 and CF_4 having a high global warming potential in order to clean the chamber by removing reaction products adhering to the inner wall. These PFC gases are also used in an etching step. Therefore, there is a fear that a large consumption of the PFC gases will cause environmental pollution. The PFC gases are used in different ways, that is, cleaning and etching, and are used for the same purpose, that is, removing.

[0007]

It is presumed that the following components of the vacuum system cause an increase in energy consumption: load-lock chambers each used for conveying a work-piece from an atmospheric environment to a vacuum environment, and a plurality of dry pumps and turbo-pumps for subjecting the process chamber to a vacuum. The following factors also cause the increase in energy consumption: an increase in footprints due to the multiplication of process chambers in order to increase the through-put, an increase in the area of the clean room because of the increase in the footprints, and an increase in the scale of the utility system for allowing the above components to work.

[0008]

In order to solve the above problems, it is an object of the present invention to provide a method for forming a pattern in which the energy consumption of a manufacturing system is reduced and PFC gases are not used, and to provide a semiconductor device.

[0009]

[Means for Solving the Problems]

The present invention is based on the following concept: when a technique for filling a recessed portion is used in order to form wiring instead of another technique for removing a layer under a mask by an etching method, a filling material in a liquid state is readily applied into the recessed portion and such a treatment can be performed under atmospheric pressure, wherein the recessed portion includes a groove or a hole formed by a mask patterning method.

[0010]

A method for forming a pattern according to Claim 1 includes the steps of forming an organic layer on a surface of a work-piece, forming a recessed portion having a predetermined pattern in the organic layer, filling the recessed portion with an inorganic material, removing the inorganic material except for the part where the inorganic material is located in the recessed portion, and removing the organic layer to allow the pattern comprising the inorganic material to remain. In the method for forming a pattern according to Claim 1, all the above steps can be performed under atmospheric pressure or a pressure near atmospheric pressure. Therefore, it is not necessary to use a vacuum system, and it is thus possible to save energy consumed in operating the system. Since a step of providing a material into a recessed portion or filling a recessed portion with a material is employed instead of another step of removing a material formed on a surface of a work-piece, the use of PFC gases used in conventional methods is not necessary.

[0011]

In a method for forming a pattern according to Claim 2, the filling of the recessed portion with the inorganic material is performed by applying a solution containing the inorganic material into the recessed portion. According to the method of forming a pattern of Claim 2, since the inorganic material has fluidity, the recessed portion is surely filled and the organic layer is surely covered with the inorganic material.

[0012]

In a method for forming a pattern according to Claim 3, the inorganic material is in a liquid phase or in a gas-liquid mixed phase. According to the method of forming a pattern of Claim 3, the inorganic material can readily be applied onto the work-piece under atmospheric pressure. When the inorganic material is in a liquid-vapor mixed state, the composition of a layer to be formed can be changed by adding a gas.

[0013]

In a method for forming a pattern according to Claim 4, the application of the inorganic material is performed by a spin coating method. According to the method for forming a pattern of Claim 4, the inorganic material can uniformly be applied onto the surface of the work-piece using centrifugal force and the recessed portion can be surely filled with the inorganic material.

[0014]

In a method for forming a pattern according to Claim 5, the application of the inorganic material is performed by a spraying method. According to the method for forming a pattern of Claim 5, since the inorganic material can be sprayed onto the organic layer with a desired pressure, the recessed portion is surely filled with the inorganic material.

[0015]

In a method for forming a pattern according to Claim 6, the removal of the inorganic material except for the part where the inorganic material is located in the recessed portion is performed by applying an etching solution. According to the method for forming a pattern of

Claim 6, since the etching solution has fluidity, the etching solution can be spread over the surface of the inorganic material so that the entire surface of the inorganic material is surely etched.

[0016]

In a method for forming a pattern according to Claim 7, the etching solution is in a liquid phase or in a gas-liquid mixed phase. According to the method for forming a pattern of Claim 7, the etching solution can be readily applied onto the work-piece under atmospheric pressure. When the etching solution is in a liquid-vapor mixed state, the composition of a layer to be formed can be changed by adding a gas.

[0017]

In a method for forming a pattern according to Claim 8, the application of the etching solution is performed by a spin etching method. According to the method for forming a pattern of Claim 8, the inorganic material can uniformly be applied onto the surface of the work-piece using centrifugal force so that the etching rate is made constant.

[0018]

In a method for forming a pattern according to Claim 9, the application of the etching solution is performed by a spraying method. According to the method for forming a pattern of Claim 9, since the etching solution can be sprayed onto the inorganic material with a desired pressure, the etching solution is surely applied onto the entire surface of the inorganic material so that the etching treatment is surely performed.

[0019]

In a method for forming a pattern according to Claim 10, the removal of the inorganic material except for the part where the inorganic material is located in the recessed portion is performed by a CMP method. According to the method for forming a pattern of Claim 10, since the inorganic material can be removed uniformly and the organic layer can be removed under atmospheric pressure without using a vacuum system, energy consumed in operating the vacuum system can be saved.

[0020]

In a method for forming a pattern according to Claim 11, the organic layer is removed by an atmospheric pressure plasma process. According to the method for forming a pattern of Claim 11, since the organic layer can be removed under atmospheric pressure without using a vacuum system, energy consumed in operating the vacuum system can be saved.

[0021]

A semiconductor device according to Claim 12 is manufactured by any one of the above methods for forming a pattern. Accordingly, the semiconductor device with the above advantages can be obtained.

[0022]

[Description of the Embodiments]

Preferred specific embodiments of a method for forming a pattern according to the present invention will be described in detail with reference to the drawings.

FIGS. 1 and 2 are illustrations showing successive steps of a

process for processing a semiconductor wafer using a method for forming a pattern according to the present invention.

[0023]

In a process for processing a semiconductor wafer, which is a work-piece, using a method for forming a pattern according to the present invention, in order to provide a wire 14 (shown in FIG. 2) on a surface 12 of a semiconductor wafer 10 shown in FIG. 1 (1), an organic photoresist is applied onto the surface 12 to form an organic photoresist layer 16, as shown in FIG. 1 (2). After forming the photoresist layer 16, the photoresist layer 16 is exposed through a mask, not shown, to form a pattern of the wire 14 (an exposure step), and the development is performed to form a groove 18, which is a recessed portion, on a surface of the photoresist layer 16. The groove 18 is designed to have the same width as that of the wire 14.

[0024]

After providing the groove 18 to the photoresist layer 16 such that the surface 12 appears, a liquid conductive inorganic material is put into the groove 18 and is applied onto the photoresist layer 16 to solidify the material to form a conductive inorganic layer 20, as shown in FIG. 1 (3). In order to apply the conductive inorganic material onto the photoresist layer 16 so as to cover the photoresist layer 16, a spin coating method is preferably used. That is, the semiconductor wafer 10 is caused to rotate and the liquid conductive inorganic material is dropped on the center of the rotating semiconductor wafer 10. The conductive inorganic material is spread out toward the periphery by

centrifugal force to uniformly form the conductive inorganic layer 20 on the face.

[0025]

After forming the conductive inorganic layer 20 on the photoresist layer 16, an etching solution in a liquid phase or in a vapor-liquid mixed phase is applied onto the conductive inorganic layer 20 under atmospheric pressure to etch the conductive inorganic layer 20, as shown in FIG. 2 (1). In the etching of the conductive inorganic layer 20, a spin etching method is preferable. When using this method, the etching solution can be applied onto the surface of the conductive inorganic layer 20 uniformly so that the conductive inorganic layer 20 is constantly etched. The etching is controlled by time management and is performed until the conductive inorganic layer 20 remains only in the groove 18, that is, until the conductive inorganic layer 20 is removed from the surface of the photoresist layer 16. In this embodiment, the removal of the conductive inorganic layer 20 is performed by the spin etching method. However, the removal is not limited to this method and other methods including, for example, a CMP method, may be used. When the conductive inorganic layer 20 is removed by the CMP method, the removal can be performed in atmosphere in the same manner as in the spin etching method. The top of the conductive inorganic layer 20 in the groove 18 can be planarized by the CMP method.

[0026]

After performing etching until the conductive inorganic layer 20 remains only in the groove 18 as described above, the resulting

semiconductor wafer 10 is introduced into an atmospheric plasma system, not shown, to remove the photoresist layer 16 remaining on the surface 12 of the semiconductor wafer 10. By removing the photoresist layer 16 in such a way, the wire 14 comprising the conductive inorganic layer 20 is completed on the surface 12 of the semiconductor wafer 10. Dry etching and chamber cleaning, which are necessary in conventional manufacturing methods, are not necessary in this method. Therefore, manufacturing is possible without using PFC gases having a high global warming potential.

[0027]

The inventors have developed a method for the isolation of semiconductor elements, a process for fabricating a FET gate electrode, and a method for forming a contact between wiring layers, wherein the methods and process employ a pattern-forming method according to the present invention. The procedures of the above three examples will now be described. The same descriptions as in the above pattern-forming method will be omitted.

[0028]

[Example 1]

FIGS. 3 and 4 are illustrations each showing successive steps of a process for isolating semiconductor elements, wherein the process employs a pattern-forming method according to the present invention.

In a semiconductor wafer, it is necessary to form insulating pattern portions among element regions 24A, 24B, and 24C each having a semiconductor element to isolate elements such that the occurrence of a

short circuit is prevented among the element regions 24A, 24B, and 24C. Insulating pattern portions 26 for isolating elements are formed according to the following procedure, as shown in FIG. 3 (1). A photoresist is applied onto a substrate surface 25 to form a photoresist layer 27, which is exposed through a mask for forming the insulating pattern portions 26 and is then developed, and etching is performed to form grooves 28 in which the substrate surface 25 appears among the element regions 24A, 24B, and 24C.

[0029]

The semiconductor wafer having the grooves 28 is subjected to a spin-coating step to apply a liquid insulating material onto the surface thereof such that the grooves 28 are filled with the material, and an insulating layer 30 is then formed. This situation is shown in FIG. 3 (2). As shown in FIG. 3 (3), the insulating layer 30 is etched until the photoresist layer 27 appears by a spin etching process. As shown in FIG. 4 (1), the photoresist layer 27 is then removed with an atmospheric plasma system.

[0030]

After removing the photoresist layer 27 in the above manner, the resulting semiconductor wafer is subjected to a spin coating step to form a silicon layer 32 on the insulating pattern portions 26 comprising the insulating layer 30. After forming the silicon layer 32, the resulting semiconductor wafer is subjected to the spin etching step again to etch the silicon layer 32 until the insulating pattern portions 26 appear.

[0031]

[Example 2]

FIGS. 5 and 6 are illustrations each showing successive steps of a process for forming an FET gate electrode, wherein the process employs a pattern-forming method according to the present invention.

As shown in FIG. 5 (1), a semiconductor wafer 34 has a silicon oxide layer thereon and a source electrode and a drain electrode of a MOS-FET (both not shown) are disposed thereon. A gate electrode 40 is formed between the source and drain electrodes according to the following procedure, as shown in FIG. 5 (2). A photoresist is applied onto a substrate surface 42 to form a photoresist layer 44, which is exposed through a mask for forming the gate electrode 40 and is then developed, and etching is performed to form grooves 46 at which the substrate surface 42 appears. The groove 46 is designed to have the same width as that of the gate electrode 40.

[0032]

The semiconductor wafer 34 having the groove 46 is subjected to a spin-coating step to apply a liquid conductive inorganic material onto the surface thereof such that the groove 46 is filled with the material, and a conductive inorganic material 48 is then formed. This situation is shown in FIG. 5 (3).

[0033]

As shown in FIG. 6 (1), the conductive inorganic material 48 is etched until the photoresist layer 44 appears by a spin etching process. As shown in FIG. 6 (2), the photoresist layer 44 is removed with an

atmospheric plasma apparatus and the gate electrode 40 is then completed on a surface of an oxide film (SiO_2) on the substrate surface 42.

[0034]

[Example 3]

FIGS. 7, 8 and 9 are illustrations each showing successive steps of a process for forming contacts between wiring contacts, wherein the process employs a pattern-forming method according to the present invention.

As shown in FIG. 7 (1), a semiconductor wafer 50 has a pair of insulating pattern portions 52 for isolation. A gate electrode 54 of a MOS-FET is disposed at the center of the area between the insulating pattern portions 52. A wiring pattern for connecting a source electrode (not shown), a drain electrode (not shown), and the gate electrode 54 is formed above the MOS-FET according to the following procedure. A photoresist is applied onto the semiconductor wafer 50 to cover the insulating pattern portions 52 and the gate electrode 54 to form a photoresist layer 58. The photoresist layer 58 is exposed through a mask for forming contact holes 60 and is then developed, and etching is performed to form the contact holes 60 through which element surfaces appear.

[0035]

After forming the contact holes 60, tungsten is deposited to fill the contact holes 60 with tungsten 62, as shown in FIG. 7 (2). As shown in FIG. 7 (3), part of the tungsten 62 disposed on the photoresist layer 58 is removed by a spin etching method or CMP. The photoresist layer 58

is then removed by another etching method using another etching solution or by an atmospheric plasma method to form projections comprising the tungsten 62 located in the contact holes 60, wherein the projections extend from the surface of an element region 56. This situation is shown in FIG. 8 (1).

[0036]

After forming the projections, which comprise the tungsten 62 and extend from the surface of an element region 56, a liquid insulating material is applied to form an insulating layer 64. As shown in FIG. 8 (2), etching is performed by a spin etching process until the tungsten 62 appears at the surface.

[0037]

After performing etching until the tungsten 62 appears, a photoresist is applied onto the surface to form a photoresist layer 66. The resulting photoresist layer 66 is exposed through a mask for forming aluminum wires 74 and is then developed. As shown in FIG. 8 (3), etching is performed to form grooves 70 at which the insulating layer 64 appears.

[0038]

After forming the grooves 70, as shown in FIG. 9 (1), an aluminum layer 72 is formed such that the grooves 70 are filled. After that, the aluminum layer 72 is etched such that parts of the aluminum layer 72 on the grooves 70 remain. As shown in FIG. 9 (2), the photoresist layer 66 is removed by an atmospheric plasma process to form aluminum wires 74 on the surface of the insulating layer 64.

[0039]

[Advantages]

As described above, a method for forming a pattern includes the steps of forming an organic layer on a surface of a work-piece, forming a recessed portion having a predetermined pattern in the organic layer, filling the recessed portion with an inorganic material, removing the inorganic material except for the part where the inorganic material is located in the recessed portion, and removing the organic layer to allow the pattern comprising the inorganic material to remain. Therefore, it is possible to save energy consumed by manufacturing facilities in a patterning step and it is not necessary to use PFC gases.

[Brief Description of the Drawings]

[FIG. 1]

FIG. 1 is an illustration showing successive steps of a process for processing a semiconductor wafer, wherein the process employs a pattern-forming method according to the present embodiment.

[FIG. 2]

FIG. 2 is an illustration showing successive steps of a process for processing a semiconductor wafer, wherein the process employs a pattern-forming method according to the present embodiment.

[FIG. 3]

FIG. 3 is an illustration showing successive steps of a process for performing isolation of semiconductor elements, wherein the process employs a pattern-forming method according to the present embodiment.

[FIG. 4]

FIG. 4 is an illustration showing successive steps of a process for performing isolation of semiconductor elements, wherein the process employs a pattern-forming method according to the present embodiment.

[FIG. 5]

FIG. 5 is an illustration showing successive steps of a process for forming an FET gate electrode, wherein the process employs a pattern-forming method according to the present embodiment.

[FIG. 6]

FIG. 6 is an illustration showing successive steps of a process for forming an FET gate electrode, wherein the process employs a pattern-forming method according to the present embodiment.

[FIG. 7]

FIG. 7 is an illustration showing successive steps of a process for forming contacts between wiring layers, wherein the process employs a pattern-forming method according to the present embodiment.

[FIG. 8]

FIG. 8 is an illustration showing successive steps of a process for forming contacts between wiring layers, wherein the process employs a pattern-forming method according to the present embodiment.

[FIG. 9]

FIG. 9 is an illustration showing successive steps of a process for forming contacts between wiring layers, wherein the process employs a pattern-forming method according to the present embodiment.

[FIG. 10]

FIG. 10 is an illustration showing successive steps of a

conventional patterning process.

[FIG. 11]

FIG. 11 is an illustration showing successive steps of a conventional patterning process.

[Reference Numerals]

1: semiconductor wafer

2: wiring layer

3: resist layer

10: semiconductor wafer

12: surface

14: wire

16: photoresist layer

18: groove

20: conductive inorganic layer

24 (24A, 24B, and 24C): element regions

25: substrate surface

26: insulating pattern portion

27: photoresist layer

28: groove

30: insulating layer

32: silicon layer

34: semiconductor wafer

40: gate electrode

42: substrate surface

44: photoresist layer

46: groove

48: conductive inorganic layer

50: semiconductor wafer

52: insulating pattern portion

54: gate electrode

58: photoresist layer

60: contact hole

62: tungsten

64: insulating layer

66: photoresist layer

70: groove

72: aluminum layer

74: aluminum wire

[Name of Document] ABSTRACT

[Abstract]

[Object] To provide a pattern-forming method in which saving energy consumed by manufacturing facilities in a patterning step is possible and the use of PFC gases is not necessary.

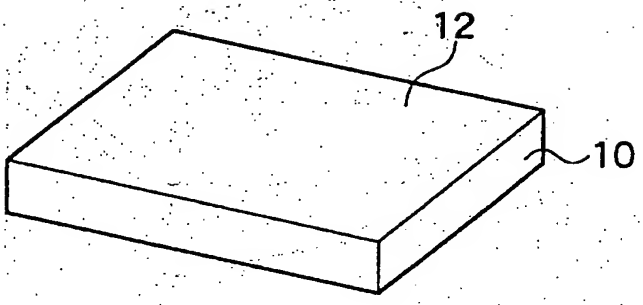
[Solving Means] A photoresist is applied onto a surface 12 of a semiconductor wafer 10 to form a photoresist layer 16, and the photoresist layer 16 is etched to form grooves 18. A conductive inorganic layer 20 is formed such that the grooves 18 are filled, and the conductive inorganic layer 20 is removed by an etching method such that parts of the conductive inorganic layer 20 in the grooves remain. After that, the photoresist layer 16 is removed to form a wire 14 comprising conductive inorganic layer 20 on a surface 12 of a semiconductor wafer 10.

[Selected Figure] FIG. 1

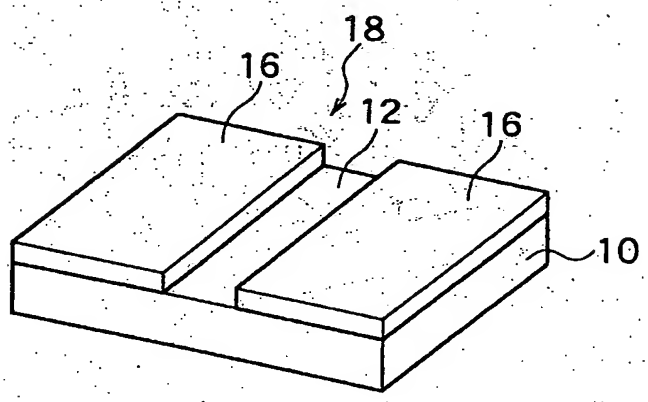
[NAME OF DOCUMENT] DRAWINGS

Fig. 1

(1)



(2)



(3)

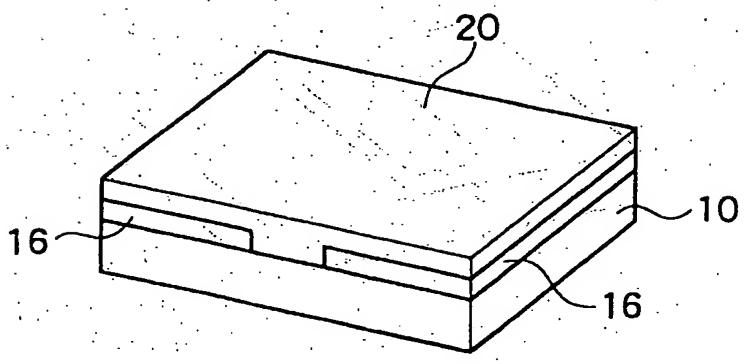
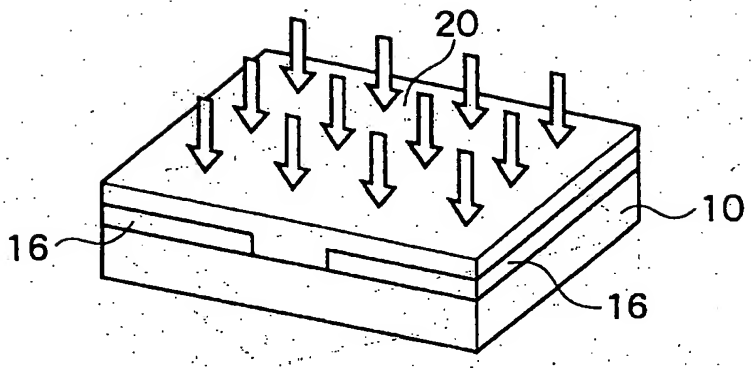
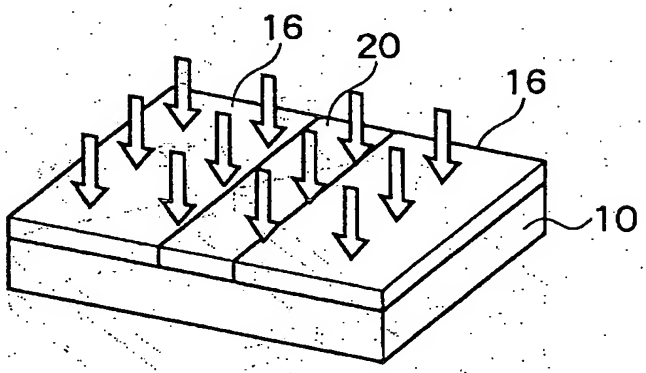


Fig. 2

(1)



(2)



(3)

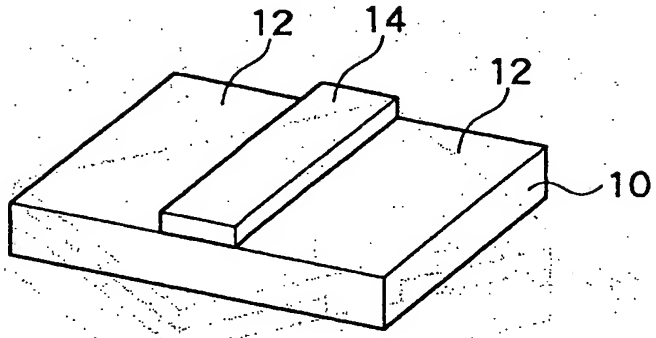
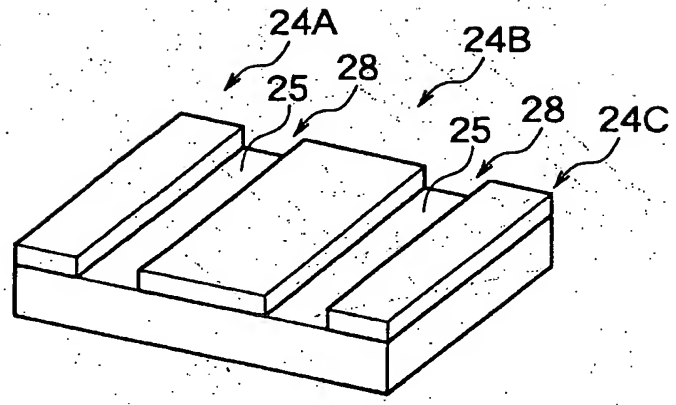
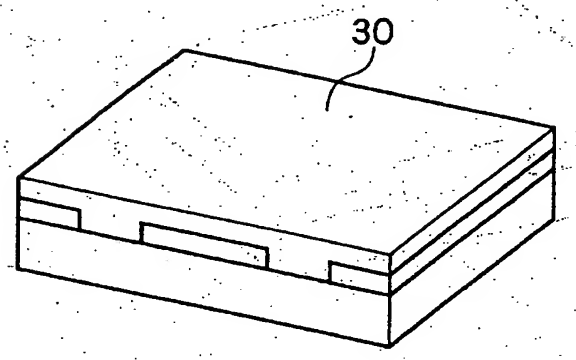


Fig. 3

(1)



(2)



(3)

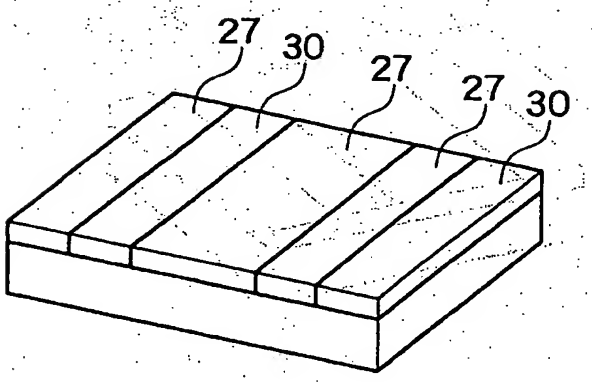
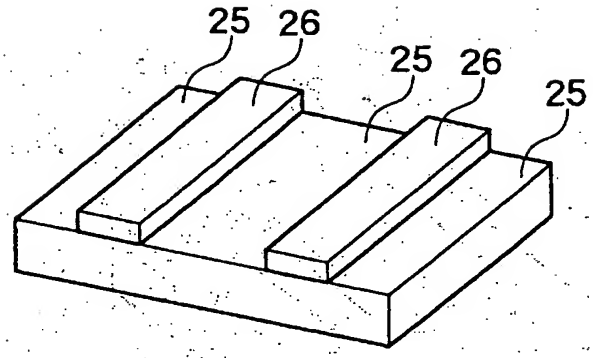
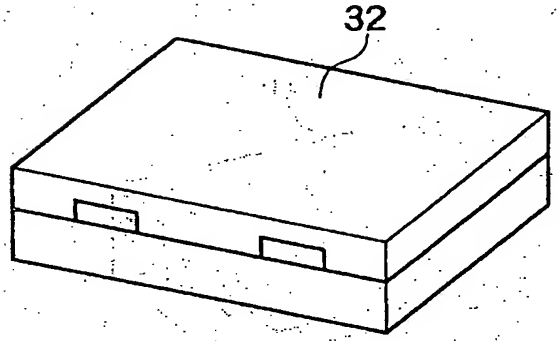


Fig. 4

(1)



(2)



(3)

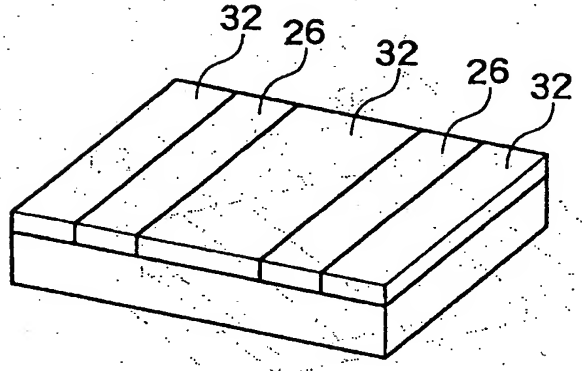
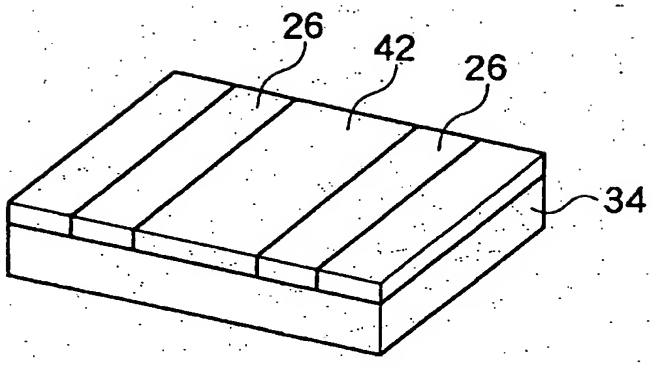
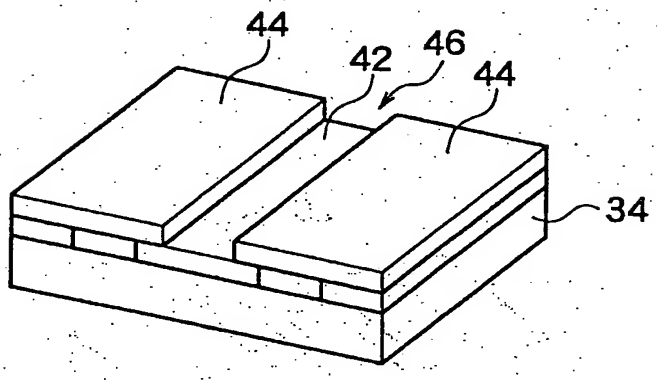


Fig. 5

(1)



(2)



(3)

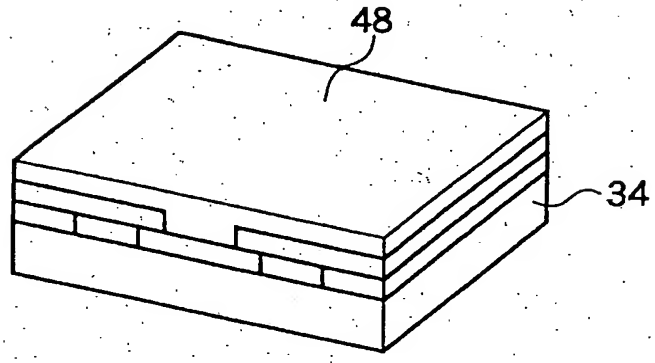
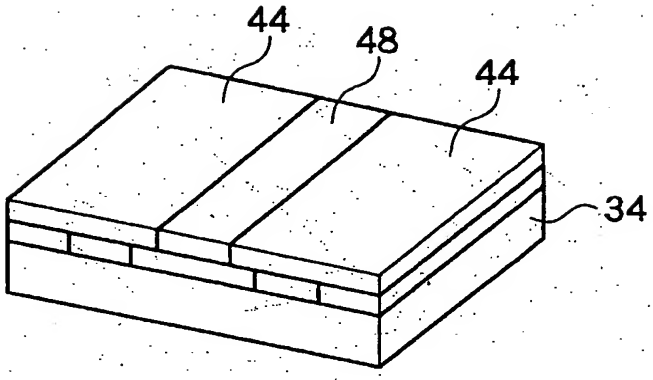


Fig. 6

(1)



(2)

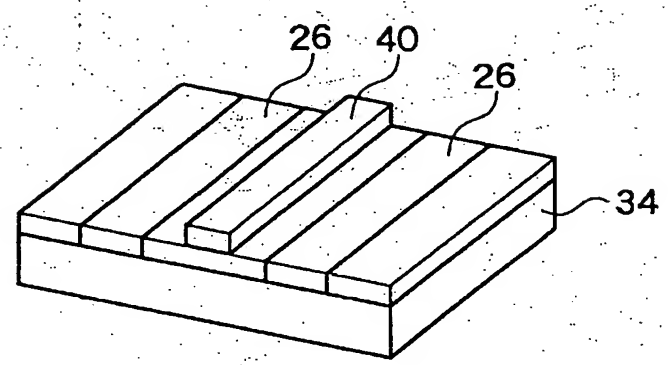
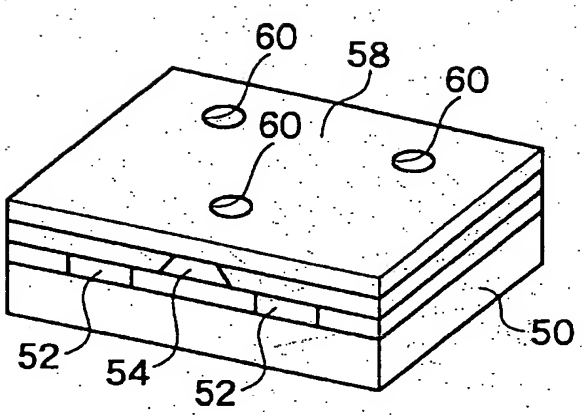
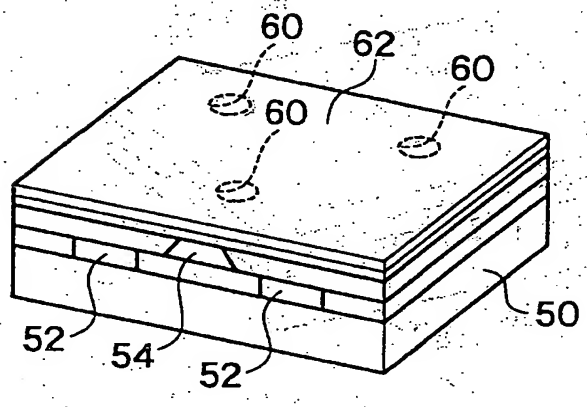


Fig. 7

(1)



(2)



(3)

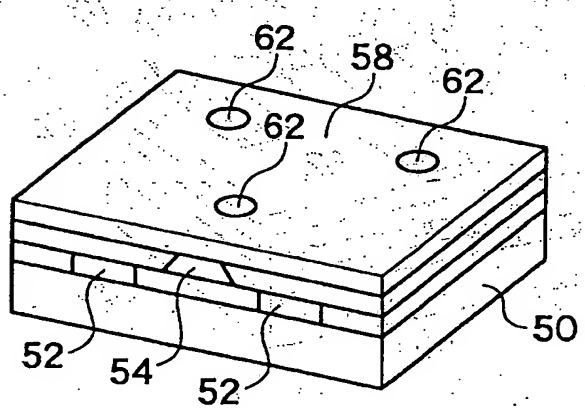
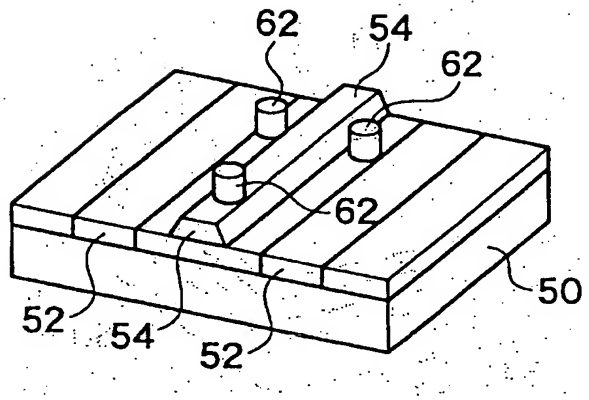
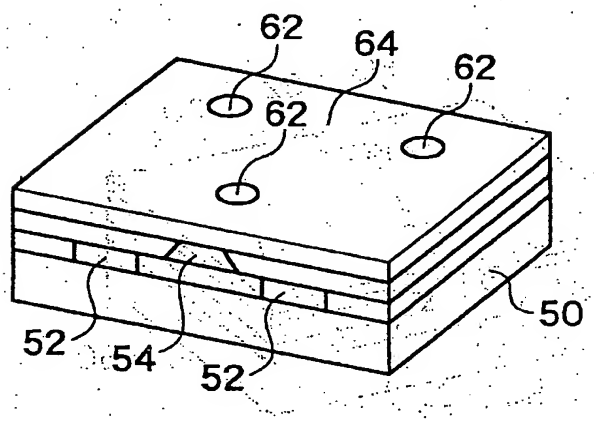


Fig. 8

(1)


62
54
62
62
52
54
52
50

(2)


62
64
62
62
52
54
52
50

(3)

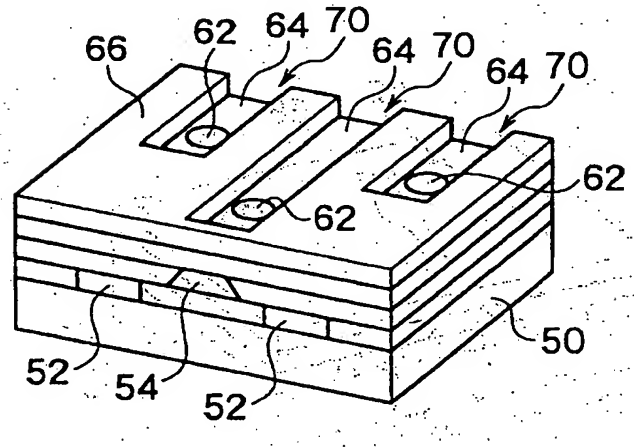
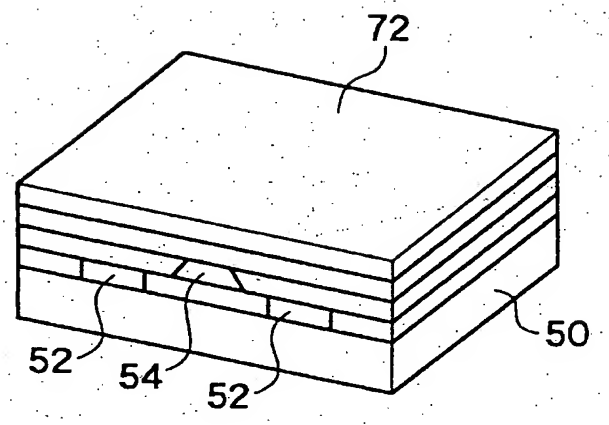

66
62
64
70
64
70
64
70
62
62
52
54
52
50

Fig. 9

(1)



(2)

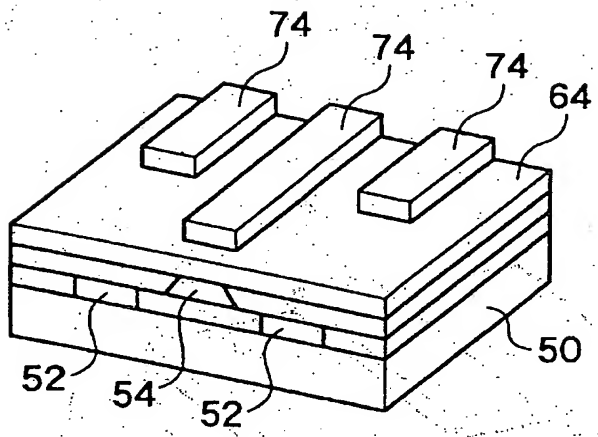
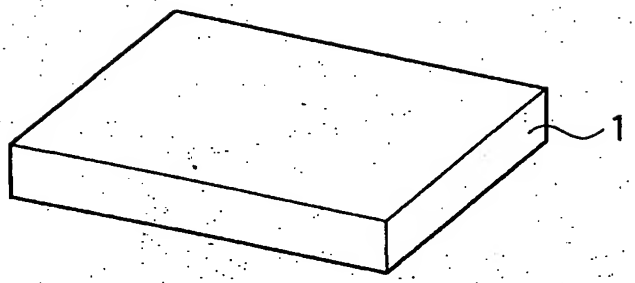
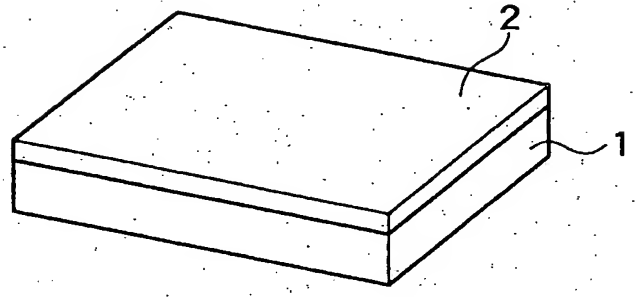


Fig. 10

(1)



(2)



(3)

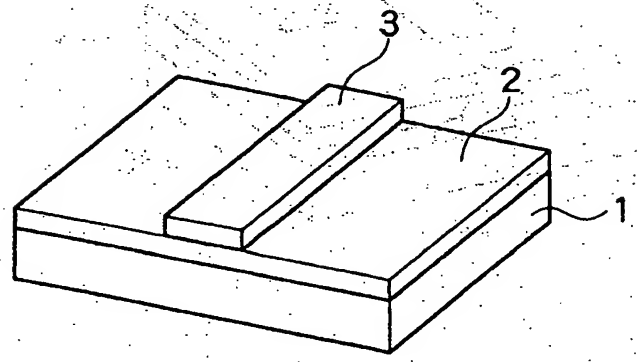
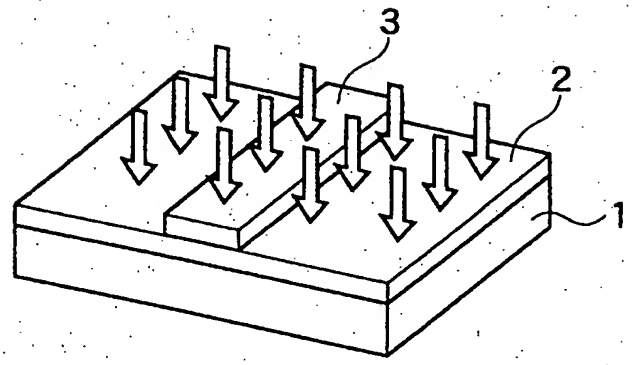
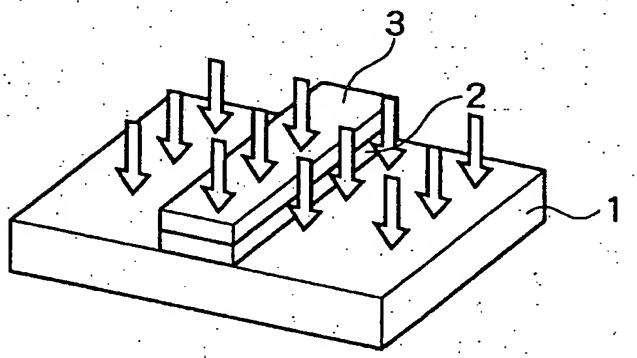


Fig. 11

(1)



(2)



(3)